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Samuels, Gauthier & Stevens LLP
Suite 3300
225 Franklin Sreet
Baston, MA 02110

EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,123	CZECH ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed on the Information Disclosure Statement filed 12/22/03. Examiner has noted that the conditions of CFR 1.97(c) are met through Applicant having paid the fee. Please find a signed copy of said Information Disclosure Statement, Form PTO-1449, enclosed with this Office Action.

Response to Amendment

Request for Reconsideration filed 12/22/03 has been forwarded to examiner on 02/06/04. Comments are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery (5,043,782) in view of Wada et al (JP361292351A), or, in the alternative: in view of Ravanelli (6,147,852). With reference to Fig. 7: Avery teaches (cf. "Field of Invention", column 1, lines 6-9) an electrostatic discharge (ESD) protective structure that protects an integrated circuit (cf. "Summary of Invention", first line) connected between a first voltage bus 20 (cf. column 4, line 27) with a first supply voltage (inherent) and a second

voltage bus or reference line 22 (cf. column 4, lines 27-28), said electrostatic discharge protective structure comprising:

a plurality of laterally designed bipolar transistors QL (cf. column 6, lines 37-42) each having a first load line connected to the first voltage bus 20 and a second line connected to the second voltage bus 22, wherein said first load lines are electrically parallel and said second load lines are electrically parallel to one another (cf. Fig. 7), each of said (laterally designed bipolar) transistors including a control connection to one of the voltage buses, namely the second voltage bus 22 (cf. Fig. 7).

Avery also teaches a resistor (RS) co-integrated into a semiconductor body preceding the control connection for one of the aforementioned laterally designed bipolar transistors QL (the one on the left in Fig. 7; cf. also column 6, lines 44-46).

Avery does not necessarily teach a single-track resistor to precede every control connection *in order to enable a large input surge voltage to be more uniformly dispersed.*

However, Wada et al teach the application of a one track resistor 2 co-integrated into the semiconductor body (cf. "Constitution", first sentence, in English abstract) *for this very purpose, i.e., in order to enable a large input voltage to be more uniformly dispersed* in an input discharge protection circuit with parallel MIS transistors, as opposed to laterally designed bipolar transistors as in the case of Avery and Applicants (see Figure 2, Abstract, and Constitution

in Wada et al). A more uniform dispersal of said large input voltage trivially lowers the breakdown voltage, providing motivation to include the teaching by Wada in the invention by Avery. However, whether or not the transistors are lateral bipolar or MIS does not appear relevant to one of ordinary skills in the art because in both cases the purpose of a more uniform dispersal of any input surge voltage is achieved through the same means as described in the claim. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Avery at the time it was made so as to include the stipulation that a single-track resistor be included as stipulated in claim 1 of Applicants.

In the alternative Ravanelli, in a patent on a ESD protection device (hence clearly analogous art; see title), teaches the inclusion of a one track resistor as Prior Art, said track resistor being co-integrated into a semiconductor body so as to precede every control connexion of a plurality of laterally designed bipolar transistors: see Figure 1 and col. 1, lines 38-45). Please note that resistor R in Figure 1 is connected to both control connexions B.

Motivation to include the teaching by Ravanelli in the invention by Avery stems from the ubiquitous advantage of "limiting the currents caused by ESDs" (Ravanelli's objective; cf. col. 1, line 45) for any ESD device including Avery's (cf. col. 1, lines 15-19), because that is what ESD protection devices are supposed to do. *Combination* of the teaching by Ravanelli and the invention by Avery is straightforward by building in the substrate according to claim 5 of Avery a resistive region (cf. col. 8, lines 4-14), which is only needed to the extent the

substrate (or P-well) has an inappropriate value for the resistivity to start with. Standard methods are available for creating resistive regions in substrates. *Success* in implementing the said combination can therefore be reasonably expected.

In summary, claim 1 is unpatentable over Avery in view of Wada et al, and, in the alternative, claim 1 is unpatentable over Avery in view of Ravanelli.

3. ***Claims 2-5*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery and Wada et al as applied to claim 1 above, and further in view of Smith (6,075,271).

With regard to claim 2: As detailed above, claim 1 (on which claim 2 depends) is unpatentable over Avery in view of Wada et al. Avery also teaches the electrostatic discharge protective structure of claim 1 wherein the semiconductor body has embedded therein at least one emitter zone and at least one collector zone (42 and 44 in Fig. 4, respectively) of first conductivity type, and at least one base zone of second conductivity type (58 in Fig. 4).

Neither Avery nor Wada et al necessarily teach a well-shaped region inserted into said semiconductor body between said zones of the first conductivity types and said base zone or zones so as to extend the path length charge carriers have to travel to the base zone.

However, the use of a deeper doped region or well to significantly increase the path length that avalanche generated charge carriers have to travel as a means to

increase the collector-to-emitter voltage in bipolar transistor dynamics is a method well known in the art, as witnessed by Smith, who teaches a deeper doped region or well-shaped region 80 (cf. abstract, lines 12-17, and Fig. 7) acting as a barrier for the avalanche-generated charge carriers involved in bipolar snap-back by blocking said charge carriers laterally, increasing the path length to be traversed by them, whereby a higher percentage of them reach the substrate 65 instead and are thus shunted to ground. Because of the specifically stipulated *motivation* as given above and the field of application, namely: technology to increase the bipolar snapback problem, it would have been obvious to one of ordinary skills in the art to modify the invention as essentially taught by Avery and Wada et al so as to include the further limitation of claim 2.

With regard to claims 3-5: the deeper doped region as taught by Smith is connected to zone 110 of first conductivity type (cf. column 4, lines 30-31 and column 7, lines 10-12) (*claim 3*) which is an electrode or source zone (cf. column 7, lines 8-9), while the examiner takes official notice that electrode or source zones intrinsically have a higher doping concentration than the other regions within the substrate (*claim 4*). The well-shaped region 80 extends more deeply into the substrate than said zone 110 to which it is attached (cf. Fig. 7).

4. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, Wada et al, and Smith as applied to claim 5 above, and further in view of Li et al (5,623,387). As detailed above, claim 5 (on which claim 6 depends) is unpatentable over Avery and Wada et al as applied to claim 1, in further view of Smith. Neither Avery,

nor Wada et al, nor Smith necessarily teach the further limitation of claim 6. However, the lateral enclosure of transistors by doped zones connected through metal contacts is well known in the art as an obvious way (creation of equipotential lines through enclosure by conductors) of creating favorable conditions for a more uniform conduction of current between emitter and collector zones in transistors, as witnessed by Li et al, who teach an esd protection circuit (cf. title) involving a bipolar transistor (cf. abstract), specifically the surrounding of first conductivity type emitter and collector zones 431, 435, by second conductivity type zones 422 connected to a common metal contact 423 (cf. Fig. 6B; see also Fig. 7B) (cf. column 13, lines 54-59). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of claim 5 so as to include the further limitation of claim 6.

5. ***Claims 7- 12*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, Wada et al, Smith, and Li et al as applied to claim 6 above, and further in view of Wong et al (6,277,689). As detailed above, claim 6 (on which claim 7 depends) is unpatentable over Avery, Wada et al, and Smith, in further view of Li et al.

Avery, Wada et al, Smith, nor Li et al, necessarily teach the further limitation defined by claim 7, except for the presence of charge carriers of the first conductivity type (see Smith, column 1, lines 37-43).

However, the use of embedded wells for the purpose of combating volatility in lateral bipolar transistors is well known in the art as witnessed by Wong who teaches a

P-well 34 embedded in an N-well 36 within a substrate 38 (cf. Fig. 4 and column 3, lines 60-64).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 6 at the time at the time of the invention so as to include the further limitation of claim 7.

With regard to claim 8: emitter and collector zones 42 and 44, respectively, as shown in Fig. 4 of Avery are designed as strips and are disposed alternatingly next to one another and parallel to one another. Thus the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: Figure 6 in Avery shows that the electrostatic discharge structure of Avery configured and arranged in an essentially square layout. Thus the further limitation of claim 9 does not distinguish over the prior art.

With regard to claim 10: the examiner takes official notice that the provision of thorough contacts between electrodes and emitter/collector regions is an obvious requirement for any transistor: without it the current through the device would be impeded and the voltage between emitter and collector would be compromised. Therefore, the further limitation of claim 10 does not distinguish over the prior art.

With regard to claim 11: The electrostatic discharge structure taught by Wada et al comprises emitter and collector electrodes connected via conductor tracks (inherent property of electrodes in any working electronics device of which they form a part) to oppositely situated voltage buses (cf. Fig. 2) and form finger-like connections (four fingers on each side in Fig. 2) which are staggered with one another so as to render as

much electrostatic balance to the configuration as possible, as indicated by the locations L1, L2, L3, and L4 in Fig. 1 in Wada et al.

With regard to claim 12: the bipolar transistor electrostatic discharge structure as taught by Avery is designed as a field oxide bipolar transistor structure, as shown by Fig. 5.

Response to Arguments

1. Applicant's arguments filed 12/22/03 have been fully considered but they are not persuasive.

In particular, Applicant alleges that the previous Office Action "abruptly concludes" obviousness (page 6, first paragraph) and is "void of any reasoning of why one of ordinary skill would have modified Avery" (page 6, third paragraph). However, examiner specifically indicates the purpose of the teaching by Wada et al of the application of one track resistor (2) as formulated on pages 4-5 of said previous Office Action, namely: for the purpose of enabling a large input surge voltage to be more uniformly dispersed (page 4, final paragraph and page 5, first paragraph). This is both a purpose of Wada as delineated in the abstract (in English as cited; "Purpose", first sentence as referred to the alteration of a polysilicon resistor; see also Figure 2 as cited in said previous Office Action), and the only aspect of the claimed invention that is lacking in Avery. Furthermore, a more uniform distribution of said large input voltage trivially lowers the breakdown voltage, breakdown being determined solely on the basis

of local conditions: minimization of the maximum in a distribution is achieved by homogenizing said distribution.

With regard to the alleged lack of proper combination (section B of Response, page 7), Wada et al may well, and in fact do indeed, disclose further alterations and specifications, in particular the said gradual decrease in channel length, however, without said further alterations and specifications, all aspects of the invention as formulated in claim 1 of Applicant are met: "causing" "uniform current flow" is not part of the invention as claimed. That Wada would not be looked at by one of ordinary skills in the art because Wada discloses channel length is not persuasive, because both Avery and Wada et al are drawn to the same art, in particular a "protection device for an integrated circuit that includes short and longer channel length structures" (Avery, first sentence of abstract), which is extremely closely related to the "input protecting circuit" achieved by "altering a polysilicon resistor and channel length" by Wada et al (English abstract). Applicant's allegation that if "the long channel length of the transistors QL were modified to include channel lengths of various sizes, then the circuit of Avery may no longer operate for its intended purpose" (lines 1-3 on page 8 of Response by Applicant) appears irrelevant to the rejection, which in no manner relies on alteration of channel length. The alleged inoperability (page 8, line 9) presumes an alteration that is neither needed nor advocated to meet claim 1.

With regard to Applicant's traverse of the rejection under 35 USC 103(a) in the alternative over Avery in view of Ravanelli that the previous Office Action is "impermissibly broad and incorrect" (final line on page 8) in citing Ravanelli, said

traverse is incorrect because an alternative to a teaching does not invalidate said teaching: pertinent to the claim language of the teachings by Ravanelli is the teaching of resistors, not of diodes, and said resistors, as admitted by Applicant on page 8, are taught to be in series, not in parallel; while the distinction between the plural resistors of Ravanelli and the singular resistor as claimed is actually one of language and not of embodiment, as witnessed by the cited portions in Ravanelli and Figure 1 accompanying said cited portions.

With regard to the traverse of the rejection under 103(a) of claims 2-5, to the extent not depending on the traverse of the rejection under 35 USC 103(a) of claim 1, Applicant's allegation that Smith "has nothing to do with ESD protective devices" is unpersuasive: see title, "Field of Invention" (lines 5-10 of col. 1), and "Background of the Invention", in which the ESD (i.e., ElectroStatic Discharge) protection is clearly stated to be the central topic of Smith's invention. That structural details of the ESD circuit not shown do not particularly matter for the ESD circuit 15 is irrelevant, because Smith had not been cited for structural details not shown but instead Smith has been cited for deeper doped region or well-shaped region 80 (see page 6 of previous Office Action). Applicant's allegation that said deeper doped region 80 "has nothing to do with an ESD device" is not persuasive because said deeper doped region 80 is both a current carrying electrode for both the first and second transistor (col. 4, l. 32-34 in Smith). Any current carrying electrode is pertinent to the ESD characteristics of the device, because breakdown is inherently caused by excess current density.

With regard to the traverse of the rejections under 35 USC 103(a) of claims 6 and claims 7-12, all arguments fall back on the traverse of the rejection of claim 1 as already discussed above.

In conclusion, regretfully the examiner must let the rejections of claims 1-12 stand.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hirata (6,469,354 B1) as provided in Information Disclosure Statement of 12/22/04.

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
April 10, 2004